**Application No.: 10/648,515** 

**IN THE CLAIMS** 

Please amend the claims as follows:

1. (Currently amended) A semiconductor memory device comprising:

a plurality of isolations formed on a semiconductor substrate;

a plurality of active regions defined on the semiconductor substrate and isolated from

each other by the isolations;

a plurality of control gate electrodes formed over the semiconductor substrate, each said

control gate electrode crossing all of the isolations and all of the active regions with a first

insulating film interposed between the control gate electrode and the semiconductor substrate;

and

a plurality of floating gate electrodes, each of which is formed for associated one of the

active regions so as to cover a side face of associated one of the control gate electrodes with a

second insulating film interposed between the floating gate electrode and the control gate

electrodes, and at least a part of each of which is formed for associated one of the active regions

so as to cover the semiconductor substrate with a third insulating film interposed between the

floating gate and the semiconductor substrate,

wherein the second insulating film includes a material different from that of the third

insulating film,

wherein the isolations are spaced apart from each other along the width of the control

gate electrodes, and

wherein each said isolation crosses all of the control gate electrodes and extends

continuously along the length of the control gate electrodes.

2

**Application No.: 10/648,515** 

2. (Original) The device of claim 1, further comprising a third insulating film formed on each of the control gate electrodes.

3. (Original) The device of claim 1, wherein each of the active regions has a plurality of step regions, each of which is overlapped by associated one of the floating gate electrodes and, wherein in each said active region, source regions are defined in respective upper parts of the step regions and a drain region is defined below the step region.

4-7. (Canceled)

8. (New) The device of Claim 1, wherein the second insulating film is formed between the upper part of the step region and the floating gate electrode.

9. (New) The device of Claim 1, wherein the second insulating film has a stacked structure of a silicon dioxide film and a silicon nitride film.